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| **DIGITAL DESIGN AND DIGITAL CIRCUITS MODELING** |
| **code**  | CSE806 |
| **title** | ΜΑΘΗΜΑ DIGITAL DESIGN AND DIGITAL CIRCUITS MODELING |
| **type (compulsory/optional)** | Optional |
| **cycle (first/second/third)** | third |
| **year of study when the component is delivered (if applicable)** | 4 |
|  **semester/trimester when the component is delivered** | 8th |
| **number of ECTS credits allocated** | 5 |
| **name of lecturer(s), with information about how, when and where to contact them.** | Stavros Souravlas, office: 425, email: sourstav@uom.edu.grOnline meeting (Google Meet, meeting can be arranged via email) |
|  **learning outcomes** | The students should be able to understand the structure of various flip-flop types and of programmable devices like PLDS, CPLDs and FPGAs and to be able to design combinational circuits (counters, sequence detectors etc). Also, they must undestand the basics of modeling and simulation of digital circuits using VHDL language |
| **mode of delivery (face-to-face/distance learning etc.)** | Face to face or distance learning |
|  **prerequisites and co-requisites (if applicable)** | Digital design basics |
| **course content** | Flip flops, counters, sequence detectors, PLDs, CPLDs, PLA, PAL, FPGA, VHDL programmable logic |
|  **recommended or required reading and other learning resources/tools** | - |
|  **planned learning activities and teaching methods** | Power Point slides, recorded lectures |
| **assessment methods and criteria** | Project |
| **language of instruction** | English |